



#F/\$
IR

PTO/SB/33 (07-05)

United States Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

58269.00014

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on _____

Signature _____

Typed or printed
Name _____

Application Number:

09/943,238

Filed: August 31, 2001

First Named Inventor:

Shrjie TZENG

Art Unit: 2616

Examiner: Moore Jr., Michael J.

Mail Stop AF

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

- ☐ Applicant/Inventor.
- ☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under
37 CFR 3.73(b) is enclosed

☒ Attorney or agent of record.
Registration No. 43,828

☐ Attorney or agent acting under 37 CFR 1.34.
Reg. No. is acting under 37 CFR 1.34 _____

Signature

Arlene P. Neal

Typed or printed name

(703) 720-7897

Telephone number

March 9, 2007

Date

NOTE: Signatures of all of the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Shrjie TZENG

Art Unit: 2616

Application No.: 09/943,238

Examiner: Moore Jr., Michael J.

Filed: August 31, 2001

Attorney Dkt. No.: 58269.00014

For: LINKED NETWORK SWITCH CONFIGURATION

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

March 9, 2007

Sir:

03/12/2007 HMARZ11 000000176 09943238
01 FC:1402

500.00 GP

In accordance with the Pre-Appeal Brief Conference Pilot Program guidelines set forth in the July 12, 2005 Official Gazette Notice, Applicant hereby submits this Pre-Appeal Brief Request for Review of the final rejections of claims 11-15 in the above identified application. Claims 1-10 and 16-23 were allowed and claims 11-15 were finally rejected in the Office Action dated November 13, 2006. Applicant filed a Response to the Final Office Action on January 16, 2007, and the U.S. Patent and Trademark Office issued an Advisory Action dated February 21, 2007 maintaining the final rejections of claims 11-15. Applicant hereby appeals these rejections and submits this Pre-Appeal Brief Request for Review. A Notice of Appeal is filed timely concurrently herewith. This Pre-Appeal Brief Request for Review is being timely filed.

Claims 11-15 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,754,216 to Wong (hereinafter Wong). As outlined below, Wong fails to disclose or suggest the elements of claims 11-15.

Wong teaches a switch fabric in communication with an Ethernet switch system. The switch fabric includes a switch processor, a memory and a FAD transceiver system for receiving and transmitting streams of cells over a high-speed data bus. The FAD transceiver includes a plurality of receive and transmit buffers, where there exists a set of buffers for every multiplex device with which the FAD is to communication. The FAD includes a logic unit, a receive

buffer, a unicast transmit buffer and a multicast transmit buffer. The Ethernet switch system includes a plurality of multiplex devices that receives and transmits data packets from the FAD system and that are coupled to a plurality of Ethernet switches that route packets to external devices connected thereto. Col. 7, line 66-Col. 8 line 36 and Figure 3 of Wong.

Wong further teaches that the switch processor communicates with the memory to obtain memory status information and to the logic unit of FAD. The switch processor controls signals to the logic unit for controlling the transmission and reception of packets and for storage and retrieval from the memory. Col. 8, lines 48-60. Figure 4 shows the switch fabric in communication with a plurality of external devices for receiving and transmitting data. As shown in figure 4, FAD include three groups of buffers, the first group being receive buffers, the second group being unicast transmit buffers and the third group being multicast transmit buffers. Col. 9, line 53-Col. 10, line 5.

Applicant submits that the rejection of claims 11-15 under 35 U.S.C. 102(e) based on the teachings of Wong is clearly erroneous. Applicants submit that Wong simply does not teach or suggest each of the elements recited in claim 11, upon which claims 12-15 depend. Claim 11, in part, recites designating **a first plurality of ports** of a first switch by a first numbering scheme, **and** designating **a second plurality of ports** of a second switch by a second numbering scheme, wherein the first plurality of ports and the second plurality of ports are configured to perform switching and rate control functions. The Office Action alleges that the first plurality of ports of the present invention is equivalent to the FAD buffers that are part of switch fabric 300 of Wong. As presented in our previous Response, as is known to those skilled in the art, a port of a switch is an interface on a switch to which other devices can be connected. A buffer, on the other hand, is known to those skilled in the art as a temporary storage area. Thus, one skilled in the art would not equate the buffers of Wong with the first plurality of port of the present invention because they are different components that perform different functions.

Col. 12, lines 28-60 of Wong disclose that the multiplex devices of figure 4 are connected to the buffers of the FAD, on one end, and, on the other end, to port interface device chips (OctaPIDs), each of which include eight port interface device that are coupled to communicate with a plurality of different Ethernet switches. Therefore, Applicant submits that even the teachings of Wong show the difference in the functions of a port and a buffer. Therefore, Wong

does not teach or suggest designating **a first plurality of ports** of a first switch by a first numbering scheme, **and** designating **a second plurality of ports** of a second switch by a second numbering scheme, wherein the first plurality of ports and the second plurality of ports are configured to perform switching and rate control functions, as recited in claim 11.

Furthermore, Applicant submits that, if as the Office Action alleges the switching fabric of Wong is equivalent to the first plurality of ports of the present invention, then there is simply no teaching or suggestion in Wong of designating **a first plurality of ports** of a first switch by a first numbering scheme, **and designating a second plurality of ports** of a second switch by a second numbering scheme, wherein the first plurality of ports and the second plurality of ports are configured to perform switching and rate control functions, as recited in claim 11, upon which claims 12-15 depend.

In the “Response to Arguments” section, the Office Action continues to allege that because “the FAD buffers of Wong are part of the switch fabric, these buffers are involved in the transmission and reception of data as well as control information between SWIP controller 414 and port interface device (OCTOPID) groups.” Therefore, according to the Office Action, the buffers of Wong are configured to perform switching and rate control functions. As is known to one skilled in the art, switching functions include examining each packet entering a port and processing it accordingly rather than simply repeating the signal to all ports. As is also known to one skilled in the art, rate control functions include controlling inputs to the switch to avoid network congestion and packet dropping.

While Wong discloses that each of FAD buffers 414-418 includes multiplexer that are used to select the specific buffer that is to transmit data SRAM memory or that is to receive data from the SRAM, there is simply no teaching or suggestion that the FAD buffers of Wong are ports that are configured to perform rate switching **and** control functions, as recited in claim 11. The Office Action alleged that Col. 15, lines 18-34 of Wong also discloses that the SWIP controller receives buffer status information from the FAD buffers and determines which FAD buffers should have their contents transmitted. Thus, the Office Action alleged that the FAD buffers perform switching functions. As noted previously, a buffer is not equivalent to a port. The Office Action also alleged that the SWIP controller transmits a congestion rating to all **port interface device** such that a determination can be made whether to transmit or discard data. Yet

the Office Action is still equating communications by the SWIP controller with FAD buffers 114-118 as communications with ports, which has been noted above to be inaccurate.

Claim 11, in part, recites designating a **first plurality of ports** of a first switch by a first numbering scheme, wherein the first plurality of ports are configured to perform switching **and** rate control functions. Applicant submits that simply because a buffer is part of a switch does not mean that the buffer is a port which is automatically configured to perform switching **and** rate control functions. Furthermore, it would not be obvious to one skilled in the art, to configure a buffer to perform switching and rate control functions. Given the arguments above, Applicant respectfully asserts that the rejection under 35 U.S.C. §102(e) is in clear error and that the rejection should be withdrawn because Wong does not teach or suggest each feature of claim 11 and hence, dependent claims 12-15 thereon.

Reconsideration and withdrawal of the rejections, in view of the clear errors in the Office Action, is respectfully requested. In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



Arlene P. Neal
Registration No. 43,828

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

APN:jkm:jf

Enclosures: PTO/SB/33 Form; Notice of Appeal; Petition for Extension of Time
Check No. 15987